UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/619,650	07/14/2003	Kyle K. Kirby	03-0301	9825

22823 7590 04/06/2005

STEPHEN A GRATTON
THE LAW OFFICE OF STEVE GRATTON
2764 SOUTH BRAUN WAY
LAKEWOOD, CO 80228

EXAMINER	
TRAN, LONG K	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 04/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/619,650	KIRBY ET AL.	
	Examiner	Art Unit	
	Long K. Tran	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-6,9-24,26 and 27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-6,9-24,26 and 27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/14/03,1/10/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of **Group I** and **Species I, claims 1, 2, 4 – 6, 9 – 24, 26** and **27** in the reply filed on January 10, 2005 is acknowledged.

2. Claims **29 – 100** have been cancelled.

3. Claims **1, 2, 4 – 6, 9 – 24, 26** and **27** are presented for examination.

Information Disclosure Statement

4. This office acknowledges of the following items from the Applicant:

Information Disclosure Statements (IDS) filed on July 14, 2003 and January 10, 2005.

The references cited on the PTO -1449 form have been considered.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims **1, 2, 4, 6, 9 – 16, 19, 26** and **27** are rejected under 35 U.S.C. 102(b) as being anticipated by Farnworth et al. (US Patent no. 5,716218).

7. Regarding claim **1**, Farnworth discloses an interconnect (fig. 1F) for a semiconductor component having a component contact comprising:

A substrate 10 (fig. 1F); and

A compliant conductive layer 45 (fig. 1F) on the substrate comprising a tip portion, covering over tip 30 of contact structure 24 (fig. 1F; col. 7, lines 8 – 19), for contacting the component contact, a shaped spring segment portion supporting the tip portion (col. 3, lines1 and 2), and a hollow interior portion 26 (fig. 1F; col. 4, lines 42 – 54) at least partially enclosed by the spring segment portion and the tip portions.

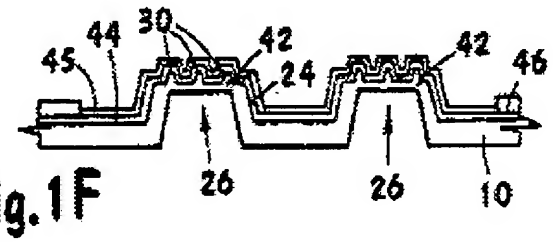

Fig. 1F

Regarding claim **2**, Farnworth discloses the shaped spring segment portion has a stepped shape open on two sides (fig. 1F).

Regarding claim **4**, Farnworth discloses the compliant conductive layer is a highly conductive metal such as aluminum (col. 7, lines 9 – 11).

Regarding claims **6** and **11**, Farnworth discloses the contact structures include needles, sharp point and bumps (col. 2, lines 3 – 6).

Regarding claim **9**, Farnworth discloses a plurality of compliant conductive layers corresponding to a plurality of component contacts on the component (col. 2, lines 28 – 31).

Regarding claim **10**, Farnworth discloses the component is contained on a semiconductor wafer comprising a plurality of components (col. 2, lines 35, 40 – 43 and 53 – 59).

Regarding claim **12**, Farnworth discloses the component contacts comprise planar pad 48 (fig. 6).

Regarding claim **13**, Farnworth discloses the component comprises a semiconductor die or a semiconductor package contained on a wafer (col. 2, lines 35, 40 – 43 and 53 – 59).

Regarding claim **14**, Farnworth discloses an interconnect (fig. 1F) for a semiconductor component having a component contact comprising:

A substrate 10 (fig. 1F); and

A compliant conductive layer 45 (fig. 1F) on the substrate having a stepped shape and a hollow interior portion 26 (fig. 1F; col. 4, lines 42 – 54), the layer having a base 44 (fig. 1F), a tip portions, covering over tip 30 of contact structure 24 (fig. 1F; col. 7, lines 8 – 19), for contacting the component contact, and spring segment portion a configured (col. 3, lines 2 and 3) to allow flexure of the tip portions (note: Farnworth does not explicitly teach the spring segment portion allowing flexure of the tip portion. However, the structure of Farnworth is similar to the structure of the claimed invention, therefore, it would allow flexure of the tip portion).

Regarding claim **15**, Farnworth discloses substrate 10 (fig. 1F) is formed of monocrystalline silicon, silicon-on-glass, silicon-on-sapphire, germanium, and ceramic (col. 4, lines 1 – 4).

Regarding claim **16**, Farnworth discloses the compliant conductive layer includes a penetrating structure for penetrating the component contact (abstract).

Regarding claim **19**, Farnworth discloses conductive traces 46 (fig. 1F; col. 7, lines 20 – 22) on the substrate in electrical communication with the compliant conductive layer.

Regarding claim **21**, Farnworth discloses a plurality of compliant conductive layers corresponding to a plurality of component contacts on the component (col. 2, lines 28 – 31).

Regarding claim **22**, Farnworth discloses the component comprises a semiconductor die or a semiconductor package contained on a wafer (col. 2, lines 35, 40 – 43 and 53 – 59).

Regarding claim **23**, Farnworth discloses an interconnect (fig. 1F) for a semiconductor component having a component contact comprising:

A substrate 10 (fig. 1F); and

A plurality of interconnect contacts (fig. 1F) on the substrate configured to electrically engage the component contacts (col. 2, lines 28 – 31), each interconnect contact comprising a base portion 44(fig. 1F) on the substrate, a shaped spring segment portion (col. 3, lines 2 and 3) on the base portion, and a tip portion, covering over tip 30 of contact structure 24 (fig. 1F; col. 7, lines 8 – 19), for contacting the component contact.

Regarding claim **24**, Farnworth discloses the component comprises semiconductor dice or a semiconductor package contained on a wafer and the

interconnect contacts are configured to electrically engage all of the component contacts (col. 2, lines 35, 40 – 43 and 53 – 59; col. 7, lines 20 – 31).

Regarding claims **26** and **27**, Farnworth discloses the shaped spring segment portion has a generally square shape (fig. 1F).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims **5, 17, 18** and **20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Farnworth et al. (US Patent no. 5,716218) in view of Gilleo et al. (US Patent no. 6,020,220).

10. Regarding claim **5**, Farnworth discloses the claimed invention of claim 1 except for the compliant conductive layer comprises a conductive polymer comprising a plurality of metal particles.

However, conductive polymer is a known material in semiconductor technology for interconnect structure as shown by Gilleo et al. (conductive polymer 190 (fig. 1A; col. 5, line 32 - 34). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to employ a well known conductive polymer in the interconnect of Farnworth as taught by Gilleo, since it has been held to be within the

general skill of a worker in the art to select a known material on the basis of its suitability for the intended use.

Regarding claims **17** and **18**, Farnworth discloses the claimed invention of claim 14 except for the compliant conductive layer comprises a conductive polymer comprising a plurality of metal particles.

However, conductive polymer is a known material in semiconductor technology for interconnect structure as shown by Gilleo et al. (conductive polymer 190 (fig. 1A; col. 5, line 32 - 34). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to employ a well known conductive polymer in the interconnect of Farnworth as taught by Gilleo, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use.

Regarding claim **20**, Farnworth discloses the claimed invention of claim 14 except for a conductive via in the substrate in electrical communication with the compliant conductive layer.

However, conductive via is known in semiconductor technology for electrical connection between layers as shown by Gilleo (a conductive via 240 (fig. 3A – 3C; col. 5, lines 59 and 60)). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to employ a well known conductive via in the substrate of Farnworth as taught by Gilleo, since it has been held to be within the general skill of a worker in the art to select a known fixture on the basis of its suitability for the intended use.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long K. Tran whose telephone number is 571-272-1797. The examiner can normally be reached on Mon-Thu.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Long Tran LKT

March 28, 2005

David Nelms
Supervisory Patent Examiner
Technology Center 2800